REMARKS

Claims 1, 4-6, 8, 9, 10, and 14 stand rejected under 35 USC §102(b) as being anticipated by Eisele, U.S. patent 6,034,995. Claims 2, 3, 7, 11, and 12 stand rejected under 35 USC §103(a) as being unpatentable over Eisele, U.S. patent 6,034,995 and Constantinescu, U.S. patent application US 2004/0252644 A1.

Claims 1, and 8 have been amended to more clearly state the invention. Claim 9 has been canceled. Reconsideration and allowance of each of the pending claims 1-8, and 10-14, as amended, is respectfully requested.

Eisele, U.S. patent 6,034,995 discloses transmission of data via a differential bus by means of balanced signals is not only reliable, but also offers the advantage that in the event of various single faults, i.e. faults concerning only one of the two lines or faults where the two lines of the differential bus are short-circuited, data transmission is still possible, be it with a reduced reliability. To this end, both lines are connected to a number of comparators which have different threshold values so that the nature of a fault occurring can be determined and, in dependence thereon, the comparator output can be determined wherefrom the recovered data signal must be derived. Column 6, lines 28-42 states:

> FIG. 2 shows the circuit for evaluating the data transmitted via the lines 11 and 12 in a station. Both lines 11 and 12 are connected to a first comparator 21 which forms the difference between the potentials on the lines 11 and 12; more exactly speaking, it subtracts the potential on the line 12 from that on the line 11 and compares the difference of correct sign with a first threshold value. This threshold value is chosen so that a low output signal is generated on the line 31 only in the recessive state of both lines 11 and 12. The line 31 is connected to a multiplexer 29 which switches the line 31 to the data output 40 in the fault-free case and in given fault cases. The line 31 is also connected to two fault detection circuits 26 and 27 which will be described in detail

hereinafter.
Column 8, lines 1-30 state:

FIG. 3 is a more detailed representation of the construction of the fault detection circuit 26 of FIG. 2. It includes two counters 51 and 54, two differentiating circuits 52 and 55 as well as two counting memories 53 and 56. The counting inputs of the counters 51 and 54 are connected together to the line 31. The input of the differentiator 52 is connected to the line 32, and the differentiator 52 outputs a brief output signal if a signal edge occurs on the line 32 due to the transition of the signal on the line 11, and the signal from the differentiator 52 resets the counter 51 to an initial position and also sets the counting memory 53 to its rest state. The differentiating circuit 55 receives the signal from the line 33 and generates, on the basis of the signal transition occurring on the line 33 in response to the transition on the line 12, a brief output signal which sets the counter 54 to an initial position and the counting memory 56 to the rest state.

If the line 11 or 12 is interrupted, signal transitions still occur on the line 31 and are counted by the two counters 51 and 54; however, depending on the interrupted line, no corresponding signal transition occurs on the line 32 or the line 33, so that the associated counter 51 or 54 is not reset but reaches a count at which the counting memory 53 or 56 is set. A fault signal is thus generated on the corresponding line 36a or 36b. Instead of using the counting memories 53 and 56, it is also possible to block the further counting by the counters when they reach the corresponding count. If the fault disappears or has been removed, a counting memory in the set state or a blocked counter is automatically reset, because in that case signal edges occur again on both lines 32 and 33.
Column 11, lines 45-63 state:

However, faults could appear or be present on the lines 11 and 12 also in the standby state of all stations, but such faults may not lead to an increased power consumption. Therefore, there is provided a fault detection circuit which is operative in the standby state and is shown in FIG. 7. Therein, the line 11 is connected to two comparators 91 and 92 which compare the potential on the line 11 with various threshold values. The comparator 91 checks whether the potential on the line 11 exceeds a value which is slightly below the supply voltage on the line 13. This is the case if the line 11 is short-circuited to the supply voltage. The signal then generated on the line 101 is applied to an input of an AND-gate 96 via a delay member 95. The output of said gate is connected to the switch 76 in FIG. 5 and isolates the resistor 14 from ground, so that in the fault case no current can flow from the supply voltage via the resistor 14 or the resistors 14 in all stations, because all stations detect the same fault and isolate the resistor 14 from ground.

Constantinescu, U.S. patent application US 2004/0252644 A1 discloses a receiver that can receive from an interconnect information packets and idle packets,

where one or more of the idle packets includes a test pattern. A condition detector can detect a condition of the interconnect in response to the test pattern. Constantinescu states:

[0021] Component 202 includes drivers 208, test pattern generator 210, encoder/decoder 212, and leaky bucket 214. Drivers 208 could include drivers using GTL (Gunning Transistor Logic), differential signaling drivers, and/or differential signaling drivers such as Low Voltage Differential Signaling Drivers (LVDs), for example. Test pattern generator 210 produces a test pattern which may be included in idle packets transmitted by component 202 via interconnect 206. According to some embodiments the test pattern produced by test pattern generator 210 may be a stress pattern selected to stress the interconnect more than regular information such as data and/or control transmitted via the interconnect. Encoding/decoding may be performed by encoder/decoder 212 using, for example, either cyclical redundancy check (CRC) or error correcting codes (ECC). Alternatively or in addition to CRC and/or ECC, errors within the idle packet may also be detected by checking the received packet against a known stress pattern. (Emphasis added)

[0028] After the information packet is sent at 308 a decision is made at 310 to determine if a transaction has successfully completed. Successful completion of a transaction may be confirmed, for example, by the return of data (such as in the case of read commands) or an acknowledge message (such as in the case of write commands). If a successful transaction has completed as determined at 310 flow can then return, for example, to check information queues at 302. However, if a successful transaction has not completed as determined at 310, failed transactions may be retried, for a predefined number of times at 312 and 314. If a retry limit is exceeded at 312 a failed interconnect flag may be set at 316. If the retry limit is not exceeded at 312 the transaction may be retried at 314, after which a determination may be made at 310 again to see if the retried transaction is successful. After a failed interconnect flag is set at 316 when the retry limit is exceeded at 312, an error handling routine may be entered at 318. After error handling, control can be transferred to the system's Operating System (OS). The error handling routine entered at 318 attempts confinement of the errors induced by the failure. In this case the application or applications that initiated the uncompleted transaction or transactions have to be terminated. If the operating system is affected by the interconnect failure a system crash occurs. FIG. 4 illustrates a flow diagram 400 representing error detection and failure prediction at a receiver. This can help signal an interconnect failure and lead to avoidance of a crashed system, for example. The flow illustrated in FIG. 4 according to some embodiments may be implemented using, for example, a component such as any of those illustrated in other drawings herein (for example by any of the processors 102, switch 104, memory controllers 110 or I/O controllers 114 illustrated in FIG. 1 or any of the components 202 and 204 illustrated in FIG. 2 or by any other components illustrated herein in later FIGS.). However, the embodiments illustrated in FIG. 4 need not be limited to being

performed by such components and need not perform exactly the same flow as illustrated in FIG. 4. Many variations of the flow illustrated in FIG. 4 may be implemented according to some embodiments. An example of where error detection and failure prediction of an interconnect failure may be implemented is in some embodiments using CRC.

[0032] If a failure is determined at 412 then a failure prediction flag is set at 414, for example, if a predefined number of errors are accumulated over a given period of time. After the failure prediction flag is set at 414 an error handling routine 416 may be used to start a process of isolating the interconnect. The interconnect may be isolated, for example, by notifying the operating system, activating a spare interconnect if one is available or finding a degraded configuration, querying the traffic over the interconnect, and/or disabling the drivers. The isolation process may be platform, firmware and operating system specific for a variety of different embodiments. Once the error handling routine 416 has finished control may be transferred to the operating system, for example. (Emphasis added)

Applicants respectfully submit that each of the pending claims 1-14, as amended, is patentable over the references of record, including Eisele and Constantinescu.

Independent claim 1, as amended, recites a method for implementing a redundancy enhanced differential signal interface. The recited method of the present invention includes the steps of providing a differential signaling I/O pair connected to a differential receiver interface; detecting an error from said differential receiver interface; responsive to said detected error, reducing an interface operating speed of said differential receiver interface; alternately testing of true and complement sides of a said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed of said differential receiver interface.

Independent claim 8, as amended, recites apparatus for implementing a

redundancy enhanced differential signal interface. The recited apparatus comprising a differential signaling I/O pair; a differential receiver interface coupled to said differential signaling I/O pair; said differential receiver interface including a pair of multiplexers coupled to a differential receiver, each multiplexer having a first input receiving a respective true or complement signal and a second input connected to a voltage reference and a multiplexer control input; and each multiplexer providing a respective true or complement output signal to said differential receiver; error detecting means coupled to said differential receiver interface for detecting an error; test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed; and alternately enabling said multiplexer control input of said pair of multiplexers for testing of true and complement sides of said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, for setting the detected failed true side or complement side of said differential receiver to a reference voltage for continued operation; and said test and failure control logic maintaining said reduced interface operating speed for continued operation after setting the detected failed true side or complement side to a reference voltage.

Eisele discloses in order to prevent brief disturbance signals on the lines from unduly switching back the memory, the first memory in each first station is preferably also coupled, via a second delay member having a second delay time, to the first comparator output in such a manner that the first memory switches over the switch

in such a manner that the data output is switched back from the second comparator output to the first comparator output if the output signal on the first comparator output does not have the first value for a period of time corresponding to the second delay time.

Eisele fails to suggest the steps of providing a differential signaling I/O pair connected to a differential receiver interface; detecting an error from said differential receiver interface; responsive to said detected error, reducing an interface operating speed of said differential receiver interface, as taught and claimed by Applicants.

The fact remains that there are significant differences between what is disclosed in the Eisele patent and the rejected claims so that it is inappropriate for the Examiner to have rejected claims 1 and 8 of the above-identified application under 35 U.S.C. §102 because "[i]t is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention" (Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379, 231 USPQ 81, 90 (Fed. Cir. 1986)). See also In re Bond, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) ("'every element of the claimed invention must be identically shown in a single reference.'").

The total teachings of Eisele and Constantinescu as set forth above, fail to suggest the steps of providing a differential signaling I/O pair connected to a differential receiver interface; detecting an error from said differential receiver interface; responsive to said detected error, reducing an interface operating speed of said differential receiver interface.

Neither Eisele nor Constantinescu suggest the step responsive to said detected error, reducing an interface operating speed of said differential receiver interface, as taught and claimed by applicants. Neither one of Eisele nor Constantinescu, and considering the total teachings in combination, suggest the step of responsive to detecting a failure of a true side or a complement side, setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed of said differential receiver interface.

Applicants respectfully submit that Eisele nor Constantinescu, considering the total teachings in combination, clearly fail to anticipate or render obvious the claimed invention. Applicants respectfully submit that Eisele nor Constantinescu, considering the total teachings in combination, fail to suggest the subject matter and the above recited steps of the present invention as set forth in independent claim 1, as amended. Thus, independent claim 1, as amended, is patentable.

Applicants respectfully submit that claim 8 is patentable for reasons as set forth with respect to claim 1. Only applicants teach that when an error is detected, an interface operating speed is reduced in response to the detected error.

The total teachings of Eisele and Constantinescu as set forth above in detail, fails to suggest error detecting means coupled to said differential receiver interface for detecting an error; test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed; and alternately enabling said multiplexer control input of said pair of multiplexers for

testing of true and complement sides of said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, for setting the detected failed true side or complement side of said differential receiver to a reference voltage for continued operation and maintaining the reduced interface operating speed, as recited in independent claim 8, as amended. Constantinescu adds nothing to render obvious the subject matter of independent claim 8, as amended.

Applicants respectfully submit that Eisele and Constantinescu, considering the total teachings in combination, clearly fail to render obvious the claimed apparatus for implementing a redundancy enhanced differential signal interface as recited in independent claim 8, as amended. Thus, independent claim 8, as amended, is patentable.

Dependent claims 2-7, and 10-14 respectively depend from patentable claims 1, and 8, further defining the invention. Each of the dependent claims 2-7, and 10-14, as amended, is likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-8, and 10-14, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application,

the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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